In The Claims:

Please amend the claims as follows:

Claim 1 (currently amended) A control chip with a bus cycle inhibiting function for preventing internal bus cycle type of the control chip, picked up from a first bus, from being re-transmitting to a second bus, the first bus and the second bus both coupled to [[~~of~~]] the control chip, the control chip comprising:

a bus cycle inhibiting circuit for receiving a bus cycle from the first bus and outputting an inhibiting signal once the bus cycle is determined to be an internal bus cycle type of the control chip, the bus cycle inhibiting circuit comprising:

a bus resource decode circuit for receiving the bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle type of the control chip, the bus resource decode circuit comprising:

an input/output resource decode unit for receiving the bus cycle from the first bus and outputting the indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle; and

a logic circuit for outputting the inhibiting signal according to a preset enable value and the indicator signal; and

a bus bridging circuit coupled to the bus cycle inhibiting circuit for inhibiting the re-transmission of the bus cycle on receiving the inhibiting signal.

Claim 2 (canceled)

Claim 3 (currently amended) The control chip of claim [[~~2~~]] 1, wherein the bus resource decode circuit comprises:

~~an input/output resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle;~~

a memory resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal memory bus cycle when the bus cycle is determined to be an internal memory bus cycle; and

a configuration resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal configuration bus cycle when the bus cycle is determined to be an internal configuration bus cycle.

Claim 4 (currently amended) The control chip of claim [[~~2~~]] 1, wherein the logic circuit comprises AND gates and OR gates.

Claim 5 (currently amended) The control chip of claim [[~~2~~]] 1, wherein the preset enable value is stored inside a register.

Claim 6 (original) The control chip of claim 1, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

Claim 7 (original) The control chip of claim 1, wherein the control chip comprises a South-bridge control chip.

Claim 8 (currently amended) A bus cycle inhibiting circuit for a control chip ~~having~~ at least coupled to a first bus and a second bus, comprising:

a bus resource decode circuit for receiving a bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle, the bus resource decode circuit comprising:

an input/output resource decode unit for receiving the bus cycle from the first bus and outputting the indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle; and

a logic circuit for outputting [[~~the~~]] an inhibiting signal according to a preset enable value and the indicator signal.

Claim 9 (currently amended) The bus cycle inhibiting circuit of claim 8, wherein the bus resource decode circuit comprises:

~~an input/output resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle;~~

a memory resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal memory bus cycle when the bus cycle is determined to be an internal memory bus cycle; and

a configuration resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal configuration bus cycle when the bus cycle is determined to be an internal configuration bus cycle.

Claim 10 (original) The bus cycle inhibiting circuit of claim 8, wherein the logic circuit furthermore comprises AND gates and OR gates.

Claim 11 (original) The bus cycle inhibiting circuit of claim 8, wherein the preset enable value is stored inside a register.

Claim 12 (original) The bus cycle inhibiting circuit of claim 8, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

Claim 13 (original) The bus cycle inhibiting circuit of claim 8, wherein the control chip comprises a South-bridge control chip.

Claim 14 (currently amended) A method of inhibiting the bus cycles of a control chip ~~having~~ at least coupled to a first bus and a second bus, comprising:

receiving a bus cycle from the first bus and determining if the bus cycle is an internal bus cycle type of the control chip, and outputting an inhibiting signal if the bus cycle is an internal bus cycle type of the control chip; and

inhibiting the re-transmission of the bus cycle to the second bus according to the actual state of the inhibiting signal.

Claim 15 (currently amended) The bus cycle inhibiting method of claim 14, wherein the inhibiting signal is issued when the bus cycle is found to be [[~~an~~]] the internal input/output bus cycle, [[~~an~~]] the internal memory bus cycle or [[~~an~~]] the internal configuration bus cycle.

Claim 16 (original) The bus cycle inhibiting method of claim 15, wherein a preset enable value is also referenced before issuing the inhibiting signal.

Claim 17 (original) The bus cycle inhibiting method of claim 14, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

Claim 18 (original) The bus cycle inhibiting method of claim 14, wherein the control chip comprises a South-bridge control chip.